

CLAIMS:

1. A method of translating an electronic design of an integrated circuit into circuit description language, comprising:
 - identifying a connection among circuit descriptions representing behavior of circuit elements in the electronic design;
 - associating an identifier with the connection; and
 - translating the electronic design into a circuit description language representation, wherein the connection is implemented within the circuit description language representation using the identifier.
2. The method of claim 1, further comprising repeating the identifying and the associating for additional connections, wherein the additional connections are implemented within the circuit description language representation using respective identifiers.
3. The method of claim 1, wherein the associating comprises relating ports associated with the connection to the identifier.
4. The method of claim 3, wherein the circuit elements are organized over levels of hierarchy, and wherein the connection among the ports spans a plurality of the levels of hierarchy.
5. The method of claim 4, wherein the circuit description language representation is organized over levels of hierarchy, and wherein the translating comprises:
 - locating ports to be connected within the electronic design based on the identifier; and

adding constructs to a plurality of the levels of hierarchy of the circuit description language representation to effect the connection among the ports located.

6. A method of translating an electronic design of an integrated circuit into circuit description language, comprising:

identifying an implicit circuit description representing behavior of a first portion of circuit elements within the electronic design;

augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with an additional circuit description; and

translating the electronic design into a circuit description language representation.

7. The method of claim 6, wherein the augmenting comprises:

identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions;

adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection; and

associating an identifier with the ports added.

8. The method of claim 7, wherein the translating comprises

locating at least two ports to be connected within the electronic design based on the identifier; and

adding constructs to the circuit description language representation to effect the connection among the at least two ports.

9. The method of claim 8, wherein the explicit circuit descriptions and the implicit circuit description are organized over levels of hierarchy within the electronic

design, and wherein the connection spans a plurality of the levels of hierarchy.

10. The method of claim 6, further comprising repeating the identifying and the augmenting for at least one additional implicit circuit description.

11. An apparatus for translating an electronic design of an integrated circuit into circuit description language, comprising:

means for identifying an implicit circuit description representing behavior of a first portion of circuit elements within the electronic design;

means for augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with an additional circuit description; and

means for translating the electronic design into a circuit description language representation.

12. The apparatus of claim 11, wherein the means for augmenting comprises:

means for identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions;

means for adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection; and

means for associating an identifier with the ports added.

13. A computer readable medium having stored thereon instructions that, when executed by a processor, cause the processor to perform a method of translating an electronic design of an integrated circuit into circuit

description language, the method comprising:

identifying an implicit circuit description representing behavior of a first portion of circuit elements within the electronic design;

augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with an additional circuit description; and

translating the electronic design into a circuit description language representation.

14. The computer readable medium of claim 13, wherein the augmenting comprises:

identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions;

adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection; and

associating an identifier with the ports added.

15. A system for translating an electronic design of an integrated circuit into circuit description language, the system comprising:

a processing unit having access to one or more storage devices;

at least a portion of the one or more storage devices having a plurality of circuit descriptions representing behavior of circuit elements of the electronic design;

at least another portion of the one or more storage devices having a program product configured to:

identify an implicit circuit description within the electronic design;

augment explicit circuit descriptions within the electronic design with an additional circuit description; and

translate the electronic design into a circuit description language representation.

16. The system of claim 15, wherein the program product is further configured to:

identify a connection among the implicit circuit description and at least one of the explicit circuit descriptions;

add ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection; and

associate an identifier with the ports added.

17. The system of claim 16, wherein the program product is further configured to:

locate at least two ports to be connected within the electronic design based on the identifier; and

add constructs to the circuit description language representation to effect the connection among the at least two ports.

18. A system for translating an electronic design of an integrated circuit into circuit description language, the system comprising:

an input section for providing electronic design data responsive to the electronic design;

an augmentation section for identifying an implicit circuit description within the electronic design data and augmenting explicit circuit descriptions within the electronic design data with an additional circuit description; and

a translation section for translating the electronic design data into a circuit description language representation.

19. The system of claim 18, wherein the translation section is further configured to:

identify a connection among the implicit circuit description and at least one of the explicit circuit descriptions;

add ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection; and

associate an identifier with the ports added.

20. The system of claim 19, wherein the translation section is further configured to:

locate at least two ports to be connected within the electronic design based on the identifier; and

add constructs to the circuit description language representation to effect the connection among the at least two ports.

21. A method for producing a circuit description language representation of an electronic design of an integrated circuit, comprising:

identifying a plurality of ports which need to be connected together;

associating with a first port of the plurality of ports a hierarchically independent indication that the first port is connected to a second port of the plurality of ports; and

connecting the first port to the second port in the circuit description language representation using the hierarchically independent indication.

22. The method of claim 21 further comprising associating with the second port of the plurality of ports the hierarchically independent indication.

23. The method of claim 22 wherein the hierarchically independent indication comprises a global identifier of the connection between the first port and the second port.